

Short Instructions for KHD2-MVI-AB2 Evaluation and Test System

1) Hardware

The KHD2-MVI-AB2 (AB2 for short) is based on the KHD2-IVI-AB1 electronics. Because the hardware has been used for over 4 years and proved to be very stable P+F was able to focus on the software aspects required to interface with the IDENT-M System V controller MVI-D2-2HRX

2) Connection

The AB2 is connected to the Remote I/O via blue hose as indicated on the side panel of the AB2. Connection between the AB2 and the IDENT-M System V controller is established via a serial cable with D-Sub connector using RS232. Terminal connections are provided if desired. Please note that the MVI-D2-2HRX utilizes the RTS and CTS signals. These signal lines must be connected to the appropriate pins on the AB2.

To facilitate communications between the AB2 and the MVI-D2-2HRX the communications parameters on the MVI-D2-2HRX need match those of the AB2 (Station Address 0, 8 data bits, 1 stop bit, No parity, 19200 baud, RTS and CTS are used). Simply set the switches SW1, SW2, SW3 and SW4 to the following setting and power up the IDENT-M System V controller. All switches are read only at power up!

SW1	Bit	1	2	3	4	5	6	7	8
SWI	Value	on	off						

CWO	Rotation	0
SW2	Position	U

SW3	Rotation	6
3443	Position	0

SW4	Bit	1	2
SW4	Value	off	off

The AB2 has two 7-position DIP switches that need to be set. The definition of those switches is as follows

Switch	1 Function	State and Description
1	System Mode	Currently not selectable. Must be set to 0
2,3	RIO Data Rate	00: 57.6kbps
		01: 115.2kbps
		10: 230.4kbps
4,5	MVI Communications	Currently not selectable. Must be set to 00
6,7	RIO Start Quarter	00: 1 st Quarter
		01: 2 nd Quarter
		10: 3 rd Quarter
		11: 4 th Quarter

Switch 2 Function

State and Description



1 RIO Last Rack 0: No

1: Yes

2-7 RIO Rack Address Binary Coded

Switch	2	3	4	5	6	7
Addresse: 0	0	0	0	0	0	0
1	0	0	0	0	0	1
2	0	0	0	0	1	0
62	1	1	1	1	1	0
63	1	1	1	1	1	1

Note: The RIO rack size of the -AB2 is fixed to quarter-rack.

3) Communication between PLC and AB2

Power up

After the -AB2 and the MVI-D2-2HRX are powered up. The -AB2 does a self diagnostic, which takes 5 seconds..

Initiating a Command - Instructing the AB2 to initiate a MVI-D2-2HRX command

Once the RIO link has been established and the RIO Scanner is in RUN mode, the green RIO LED on the AB2 is on solid. At that point the PLC can communicate with the AB2 by using BTW and BTR commands. In most cases the BTW command is followed by BTR. The combination of BTW and BTR constitutes a communication cycle. The user specifies an action by the MVI-D2-2HRX by issuing a BTW command. Instructing the ID system to read information from the data carrier, write information to the data carrier or changing the state of one of the outputs on the MVI-D2-2HRX are examples of actions initiated by BTW. The following table lists the available commands the PLC can issue via BTW.



BTW Control Word Format

	0	1	1	1	0	0	H1	H0	C3	C2	C1	C0	0	0	0	M
De	finitio [ns H1				Comn	nand i	s with	respec	ct to A	ntenn	a 1				
		H0	1 C2	C2		Comn	nand i	s with	•							
	H	M	1 C2	C3		On/O			g the s	state o	f MVl	[-D2-2	HRX	outpu	its. No	ote
						that that cl				•					ept the	e ones

Please note that the first byte can only be 70_{hex} , 71_{hex} or 72_{hex} . Depending on the antenna that is being used for the following command. System relevant commands that do not involve an antenna use 70_{hex} , commands that utilize antenna 0 start with 71_{hex} , and commands for antenna 1 start with 72_{hex} .

Command	C3	C2	C1	CO	M	Control Word
Reset MVI-D2-2HRX	1	1	1	1	*	70F0
Read AB2 Software Version	1	1	1	0	*	70E0
Set Output 1 on/off	1	1	0	0	1	70C1 Turn on Output-1 70C0 Turn off Output-1
Set Output 2 on/off	1	0	1 1	1 1	1 0	70B1 Turn on Output-2 70B0 Turn off Output-2
Set Output 3 on/off	1	0	1 1	0	1 0	70A1 Turn on Output-3 70A0 Turn off Output-3
Set Output 4 on/off	1	0	0	1 1	1 0	7091 Turn on Output-4 7090 Turn off Output-4
Initialize Data Carrier	0	1	0	1	*	7150 Initialize Data Carrier in the zone of
						Antenna 0 7250 Initialize Data Carrier in the zone of Antenna 1



Write Data Carrier

0 1 0 0 *

7140<start><length><data> -- Write the <data> string of <length> words to the Data Carrier in the zone of Antenna 0, starting at address <start>. <start> is the byte address in hex. <length> is the word length in hex and must be less than 3C_{hex} (60_{dec})

7240<start><length><data> Write the <data> string of <length> words to the Data Carrier in the zone of Antenna 1, starting at address <start>

Example: Write Data Carrier using Antenna 0 starting at byte 15_{hex} with a length of 10_{hex} words. 7150 0015 0010 {......16 Words of Data......}

Read Data Carrier

0 0 1 0 *

7120<start><length> Read a data string of <length> words from the Data Carrier in the zone of Antenna 0, starting at address <start>. <start> is the **byte address in hex**. <length> is the **word length in hex** and must be less than $3C_{\text{hex}}(60_{\text{dec}})$

7220<start><length> Read a data string of <length> bytes from the Data Carrier in the zone of Antenna 1, starting at address <start>

Example: Read Data Carrier using Antenna 0 starting at byte 100_{hex} with a length of $0A_{\text{hex}}$ words. 7120 0100 000A

Response – Instructing the AB2 to send the MVI-D2-2HRX response to the PLC BTR

The BTR command is used to transfer information buffered in the AB2 to the PLC. The information buffered in the AB2 is the response to the last BTW command. Note also that because the BTR transfers the response of the MVI-D2-2HRX to a previous BTW to the PLC a BTR must never be the first command after system power-up. (In this case the AB2 does not have any data to send back to the PLC and the PLC will time-out). When issuing a BTR you should always specify the data length as **zero**. The AB2 unit will then determine the proper number of words to send back to the PLC. Depending on the command issued by the BTW the AB2 will respond differently when data is requested by the BTR.



All valid BTR will contain a minimum of two words. The first word is the status word and therefore contains information concerning the operational status of the AB2, serial connection between MVI-D2-2HRX and the AB2, and MVI-D2-2HRX. The second word contains detailed error codes issued by the MVI-D2-2HRX (if applicable) and is called MVI Error Word. The individual bits in the status word have the following meaning.

Status1: Bit7: Always 0

Bit6: AB2 Microprocessor internal RAM error

Bit5 AB2 External RAM error

Bit4 AB2 Node Adapter Chip RAM errorBit3 MVI-D2-2HRX to AB2 serial error

Bit2 Always 0

Bit1 Low Battery in MVI-D2-2HRX

Bit0 Low Battery in MVC-60-64K Data Carrier

Status0: Bit7: Unknown Remote I/O Command received by AB1

Bit6: Remote I/O Command in progress

Bit5 Always 0 Bit4 Always 0 Bit3 Always 0

Bit2 MVI-D2-2HRX System Error Response

Bit1 Antenna 1 Active **Bit0** Antenna 1 Active

The bit value of the second response word is zero most of the time. Only if **bit 2** of **Status0** is high (1) does the second response word carry any meaning. If **bit 2** of **Status0** is high the value of the second response word is the exact error message code sent by the MVI-D2-2HRX to the AB2. Those error codes are explained in section 13.3 of the IDENT-M System V Users Manual.

In certain cases BTR will cause the AB2 to transfer additional data to the PLC. How much data is transferred depends on the BTW commands issued previously. The following examples should clarify this. "*" indicates bits that can be either 0 or 1 and indicate the status of the system or data transfer. It is also assumed that the MVI-D2-2HRX does not respond with an error message (**Status0-Bit2** = 0). Therefore the MVI Error word contains zeros only.

☐ Reset Interface: BTW 70F0

No Response – Do not issue BTR

Must wait five (5) seconds before issuing next command



☐ Read AB2 Software Version: BTW 70E0

Responds with AB2 Software Version after Status and MVI Error words

	Status1 Status0 7 6 5 4 3 2 1 0 7 6 5 4 3 2																									M	VI	Er	ror			
7	6	<u> </u>	5	4	3	2	1	0	7	6	5	4	3		1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
0	*	•	*	*	*	0	*	*	*	*	0	0	0	*	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

☐ Set/Reset Output x BTW 7091/7090

BTW 70A1/70A0 BTW 70B1/70B0 BTW 70C1/70C0

			5	Sta	tus	1					S	Stat	us	0													M	VI	En	ror		
_	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
(C	*	*	*	*	0	*	*	*	*	0	0	0	*	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

☐ Initialize Data Carrier at Antenna0 BTW 7150

	7 6 5 4 3 2 1 0 7 6 5 4 3 2																								M	VI	En	ror			
7	6	5	4	3	2	1	0	7	6	5	4	3		1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
0	*	*	*	*	0	*	*	*	*	0	0	0	*	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

...... Antenna1 BTW7250

		S	Sta	tus	1					S	Stat	us	0													M	VI	En	ror		
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
0	*	*	*	*	0	*	*	*	*	0	0	0	*	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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☐ Write Data Carrier at Antenna0 BTW 7140<start><length><data>

		S	Stat	us	1					S	Stat	us	0													M	VI	En	ror		
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
0	*	*	*	*	0	*	*	*	*	0	0	0	*	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

...... Antenna1 BTW 7240<start><length><data>

Status1 Status0 7 6 5 4 3 2 1 0 7 6 5 4 3 2 1																								M	VI	En	ror				
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
0	*	*	*	*	0	*	*	*	*	0	0	0	*	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

☐ Read Data Carrier at Antenna0 BTW 7120<start><length>

			S	Stat	tus	1					S	Stat	us	0													M	VI	En	ror		
Ī	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Γ	0	*	*	*	*	0	*	*	*	*	0	0	0	*	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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					I	Dat	a V	Vo	rd (0											I	Dat	a V	Wo	rd	1					
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
	7 6 5 4 3 2 1 0 7 6 5 4 3 2 1 0 Data bits requested																		D	ata	ı bi	its	rec	que	este	ed					

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..... Antenna1

BTW 7220<start><length>

		5	Stat	tus	1					S	Stat	us	0													M	VI	En	ror		
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
0	*	*	*	*	0	*	*	*	*	0	0	0	*	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
+																															
					I	D at	аV	Vo	rd (0											I) at	a V	Vo	rd	1					

					I	D at	a V	Vo:	rd ()												D at	a V	Vo	rd	1					
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
7 6 5 4 3 2 1 0 7 6 5 4 3 2 1 0 Data bits requested																		D	ata	ı bi	its	rec	que	este	ed						

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