Notes:

1. The entity concept allows interconnection of intrinsically safe and associated apparatus not specifically examined in combination as a system when the approved values of $U_o$ (or $V_{max}$) and $I_0$ (or $I_{max}$) for the associated apparatus are less than or equal to $U_i$ (or $V_{max}$) and $I_i$ (or $I_{max}$) for the intrinsically safe apparatus and the approved values of $C_0$ (or $C_{0max}$) and $C_i$ (or $C_{i max}$) for the associated apparatus are greater than $C_{i max}$ and $C_{0 max}$, respectively, for the intrinsically safe apparatus.

2. This associated apparatus may also be connected to simple apparatus as defined in Article 504.2 and installed and temperature classified in accordance with Article 504.10 (B) of National Electrical Code (ANSI/NFPA 70) or other local codes, as applicable.

3. Where multiple circuits extend from the same piece of associated apparatus, they must be installed in separate cables or in one cable having suitable insulation. Refer to Article 504.30 (3) of the National Electrical Code (ANSI/NFPA 70) and Instrument Society of America Recommended Practice ISA RP12.6 for installing intrinsically safe equipment.

4. Intrinsically safe circuits must be wired and separated in accordance with Article 504.20 of National Electrical Code (ANSI/NFPA 70) or other local codes as applicable.

5. Associated apparatus must be installed in enclosure suitable for the environment in accordance with the National Electrical Code (ANSI/NFPA 70) or other local codes as applicable.

6. Barriers shall not be connected to any device that uses or generates in excess of 250 Vrms or DC unless it has been determined that the voltage is adequately isolated from the barrier.

7. Single channel modules use either input terminals 1, 2, 3 or 4, 5, & 6.

<table>
<thead>
<tr>
<th>Mode Numbers</th>
<th>( V_{OC} )</th>
<th>( I_{SC} )</th>
<th>( C_{0max} )</th>
<th>GRPS</th>
<th>( I_{max} )</th>
<th>GRPS</th>
</tr>
</thead>
<tbody>
<tr>
<td>KT5-2R2-Ex1x</td>
<td>12.9</td>
<td>19.8</td>
<td>1.273</td>
<td>0.18</td>
<td>84.8</td>
<td>678.4</td>
</tr>
</tbody>
</table>

The values of $C_0$ and $C_i$ listed in the table above are allowed if one of the following conditions is met:

- the total \( I_i \) of the external circuit (excluding the cable) is < 1% of the \( I_0 \) value.
- the total \( C_i \) of the external circuit (excluding the cable) is < 1% of the \( C_0 \) value.

The values of $L_0$ and $L_i$ listed in the table above shall be reduced to 50% when both of the following conditions are met:

- the total \( I_i \) of the external circuit (excluding the cable) is > 1% of the \( I_0 \) value.
- the total \( C_i \) of the external circuit (excluding the cable) is > 1% of the \( C_0 \) value.

Note: the reduced capacitance of the external circuits (including cable) shall not be greater than 1uF for IIB and 600nF for IIC.