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FMEDA including SFF determination and PFD calculation

Project:

Smart Transmitter Isolators
KFD2-STC(V)4-*** and ED2-STC(V)4-***

Customer:

Pepperl+Fuchs GmbH
Mannheim
Germany

Contract No.: P+F 01/04-03D
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Management summary

This report summarizes the results of the FMEDAs carried out at the smart transmitter isolators KFD2-STC(V)4-*** and ED2-STC(V)4-***. '***' stands for the different versions that are available. Table 1 gives an overview and explains the differences.

Table 1: Version overview

Type	Current source out	Current sink out	Voltage out	Housing	Input config.	Channels
KFD2-STC4-(Ex)1	X			DIN-rail	3 wire	1 in, 1 out
KFD2-STC4-(Ex)1.2O	X			DIN-rail	3 wire	1 in, 2 out
KFD2-STC4-(Ex)2	X			DIN-rail	2 wire	2 in, 2 out
KFD2-STC4-(Ex)1-Y		X		DIN-rail	3 wire	1 in, 1 out
KFD2-STC4-(Ex)1.2O-Y		X		DIN-rail	3 wire	1 in, 2 out
KFD2-STC4-(Ex)2-Y		X		DIN-rail	2 wire	2 in, 2 out
KFD2-STV4-(Ex)1			X	DIN-rail	3 wire	1 in, 1 out
KFD2-STV4-(Ex)1.2O			X	DIN-rail	3 wire	1 in, 2 out
KFD2-STV4-(Ex)2			X	DIN-rail	2 wire	2 in, 2 out
ED2-STC4-(Ex)1	X			Euro-Card	2 wire	1 in, 1 out
ED2-STC4-(Ex)2	X			Euro-Card	2 wire	2 in, 2 out
ED2-STC4-(Ex)1-Y		X		Euro-Card	2 wire	1 in, 1 out
ED2-STC4-(Ex)2-Y		X		Euro-Card	2 wire	2 in, 2 out
ED2-STV4-(Ex)1			X	Euro-Card	2 wire	1 in, 1 out
ED2-STV4-(Ex)2			X	Euro-Card	2 wire	2 in, 2 out

The failure rates are based on the Siemens standard SN 29500.

According to table 2 of IEC 61508-1 the average PFD for systems operating in low demand mode has to be 10^{-3} to < 10^{-2} for SIL 2 safety functions. However, as the modules under consideration are only one part of an entire safety function they should not claim more than 10% of this range, i.e. they should be better than or equal to 10^{-3}.

The boards under evaluation can be considered to be Type A components.

For **Type A** components the SFF has to be 60% to < 90% according to table 2 of IEC 61508-2 for SIL 2 (sub-) systems with a hardware fault tolerance of 0.

The following two tables show which boards (considering one input and one output being part of the safety function) under which assumptions fulfill this requirement.

Table 2: Summary for the three-wire input versions[1]

Failure Categories[2]	T[Proof] = 1 year	T[Proof] = 2 years	T[Proof] = 5 years	SFF
Fail low (L) = Safe Fail High (H) = Safe	**PFD_{AVG} = 1.6E-04**	**PFD_{AVG} = 3.2E-04**	**PFD_{AVG} = 8.0E-04**	> 91 %
Fail low (L) = Safe Fail High (H) = Dangerous	**PFD_{AVG} = 2.2E-04**	**PFD_{AVG} = 4.5E-04**	**PFD_{AVG} = 1.1E-03**	> 87 %
Fail low (L) = Dangerous Fail High (H) = Safe	**PFD_{AVG} = 7.9E-04**	**PFD_{AVG} = 1.6E-03**	**PFD_{AVG} = 3.9E-03**	> 56 %
Fail low (L) = Dangerous Fail High (H) = Dangerous	**PFD_{AVG} = 8.6E-04**	**PFD_{AVG} = 1.7E-03**	**PFD_{AVG} = 4.3E-03**	> 52 %

Table 3: Summary for the two-wire input versions[3]

Failure Categories[2]	T[Proof] = 1 year	T[Proof] = 2 years	T[Proof] = 5 years	SFF
Fail low (L) = Safe Fail High (H) = Safe	**PFD_{AVG} = 1.6E-04**	**PFD_{AVG} = 3.2E-04**	**PFD_{AVG} = 8.0E-04**	> 90 %
Fail low (L) = Safe Fail High (H) = Dangerous	**PFD_{AVG} = 2.2E-04**	**PFD_{AVG} = 4.5E-04**	**PFD_{AVG} = 1.1E-03**	> 86 %
Fail low (L) = Dangerous Fail High (H) = Safe	**PFD_{AVG} = 7.3E-04**	**PFD_{AVG} = 1.5E-03**	**PFD_{AVG} = 3.6E-03**	> 56 %
Fail low (L) = Dangerous Fail High (H) = Dangerous	**PFD_{AVG} = 7.9E-04**	**PFD_{AVG} = 1.6E-03**	**PFD_{AVG} = 3.9E-03**	> 52 %

The boxes marked in yellow (🟨) mean that the calculated PFD values are within the allowed range for SIL 2 according to table 2 of IEC 61508-1 but do not fulfill the requirement to not claim more than 10% of this range, i.e. to be better than or equal to 10^{-3}. The boxes marked in green (🟩) mean that the calculated PFD values fulfill this requirement to be better than 10^{-3}. The boxes marked in red (🟥) mean that for the described configuration of fail low and fail high failures, the achieved SFF is only sufficient for SIL 1 safety functions.

The two channels on each module should not be used for one safety function as they contain common components.

[1] The results are based on the FMEDA carried out at the KFD2-STC4-Ex1 version but is considered to be representative for all KFD2-STC(V)4-… three-wire input boards.

[2] The failure categories are explained in detail in section 4.1.

[3] The results are based on the FMEDA carried out at the KFD2-STC(V)4-Ex2 version but is considered to be representative for all KFD2-STC(V)4-… and ED2-STC(V)4-… two-wire input boards.

Table of Contents

1 Purpose and Scope

This document shall describe the results of the FMEDAs carried out at the smart transmitter isolators KFD2-STC(V)4-*** and ED2-STC(V)4-***. '***' stands for the different versions that are available. Table 1 gives an overview and explains the differences.

It shall be assessed whether these boards meet the Probability of Failure on Demand (PFD) requirements for SIL 2 sub-systems according to IEC 61508. It **does not** consider any calculations necessary for proving intrinsic safety.

Pepperl+Fuchs GmbH contracted *exida.com* L.L.C. in May 2001 with the FMEDA and PFD calculation of the above mentioned boards.

2 Project management

2.1 Roles of the parties involved

Pepperl+Fuchs	Manufacturer of the smart transmitter isolators.
exida.com	Did the FMEDAs together with the determination of the Safe Failure Fraction (SFF) and calculated the Probability of Failure on Demand (PFD) using Markov models.

2.2 Standards / Literature used

The services delivered by *exida.com* were performed based on the following standards / literature.

N1	IEC 61508-2: 1999	Functional Safety of Electrical/Electronic/Programmable Electronic Safety-Related Systems
N2		Electronic Components: Selection and Application Guidelines by Victor Meeldijk John Wiley & Sons; ISBN: 0471133019
N3		Failure Mode / Mechanism Distributions FMD-91, RAC 1991
N4	SN 29500	Failure rates of components

2.3 Reference documents

2.3.1 Documentation provided by the customer

D1	KFD2-STC(V)4-Ex2…	Circuit Diagram no. 251-0316J of 01.12.00
D2	KFD2-STC(V)4-Ex1(.2O)…	Circuit Diagram no. 251-0339D of 03.11.00
D3		Parts list for KFD2-STC(V)4-Ex2…
D4	ED2-STC4-EX2	Circuit diagram no. 01-5068 of 19.12.00
D5		STC4 Reference List ED2_KFD2

2.3.2 Documentation generated by *exida.com*

R1	STC4-Ex1 5 and 10 Volt FMEDA V0 R0.1.xls
R2	STC4-Ex1 current source and sink FMEDA V0 R0.1.xls
R3	STC4-Ex2 5 and 10 Volt FMEDA V0 R0.1.xls
R4	STC4-Ex2 current source and sink FMEDA V0 R0.1.xls

3 Description of the analyzed modules

3.1 KFD2-STC(V)4-Ex1.2O

The KFD2-STC(V)4-Ex1.2O board provides a transformer isolated power supply for a transmitter located in a potentially explosive atmosphere. The transmitter may be a two-wire current sink or a two-wire current source one. The device itself must be located in the safe area. The field current drawn by the transmitter is repeated as two currents in the safe area. The safe area output signals are isolated from the power supply and from each other. The power supply and output terminals are isolated from the hazardous area terminals.

In addition to the transfer of analog current signals from the hazardous area, the unit will transfer signals in the form of an alternating current from the hazardous area or an alternating voltage from the safe area. This allows bi-directional communication between a smart transmitter located in the field and suitable equipment located in the safe area.

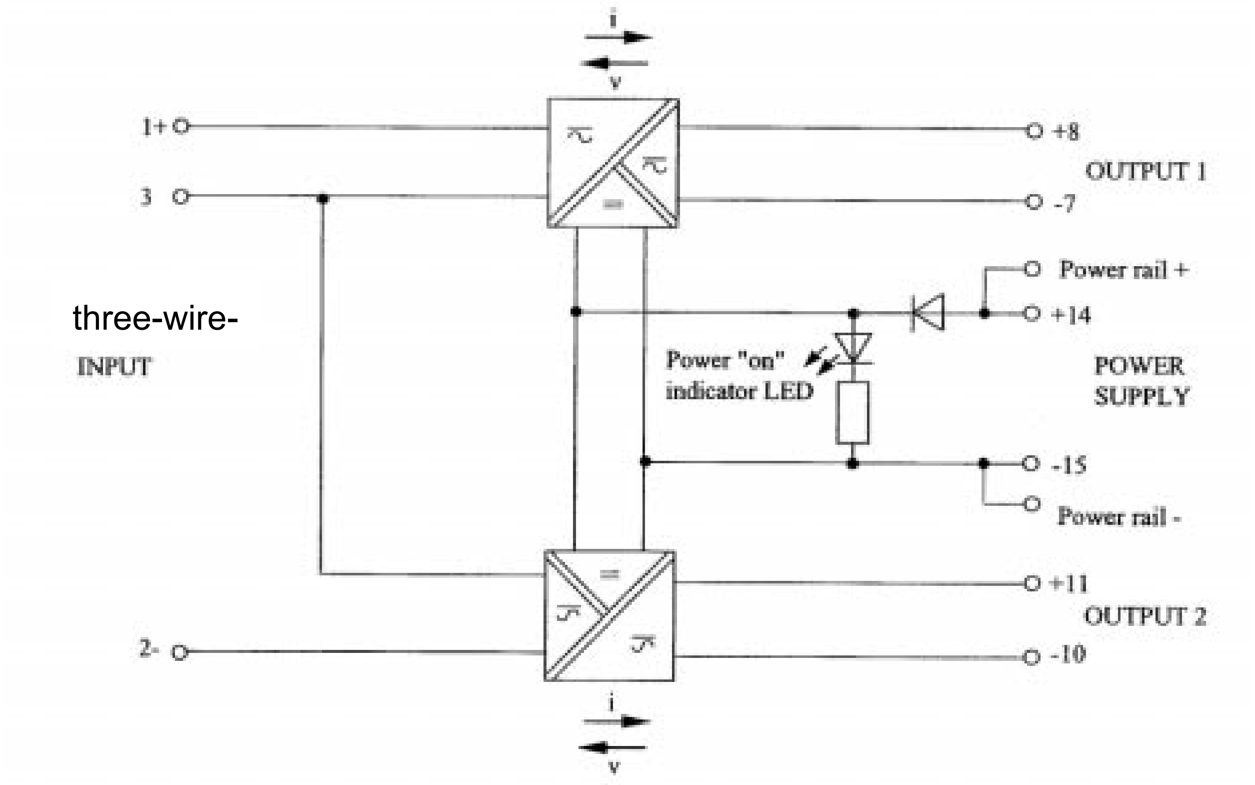


Figure 1: Block diagram of KFD2-STC(V)4-Ex1.2O

Remark: The description above is valid accordingly for all other three-wire input channel versions with the exception that this version has two output channels. The differences between the versions are described in Table 1.

3.2 KFD2-STC(V)4-Ex2

The KFD2-STC(V)4-Ex2 is a two channel transformer isolated device providing fully floating power supply for transmitters located in a potentially explosive atmosphere. The device itself must be located in the safe area. The field current drawn by each transmitter is repeated as an identical current in the safe area. The safe area output signal is isolated from the power supply but the two may be connected together externally if required. The power supply and output terminals are isolated from the hazardous area terminals.

In addition to the transfer of analog current signals from the hazardous area, the unit will transfer signals in the form of an alternating current from the hazardous area or an alternating voltage from the safe area. This allows bi-directional communication between a smart transmitter located in the field and suitable equipment located in the safe area.

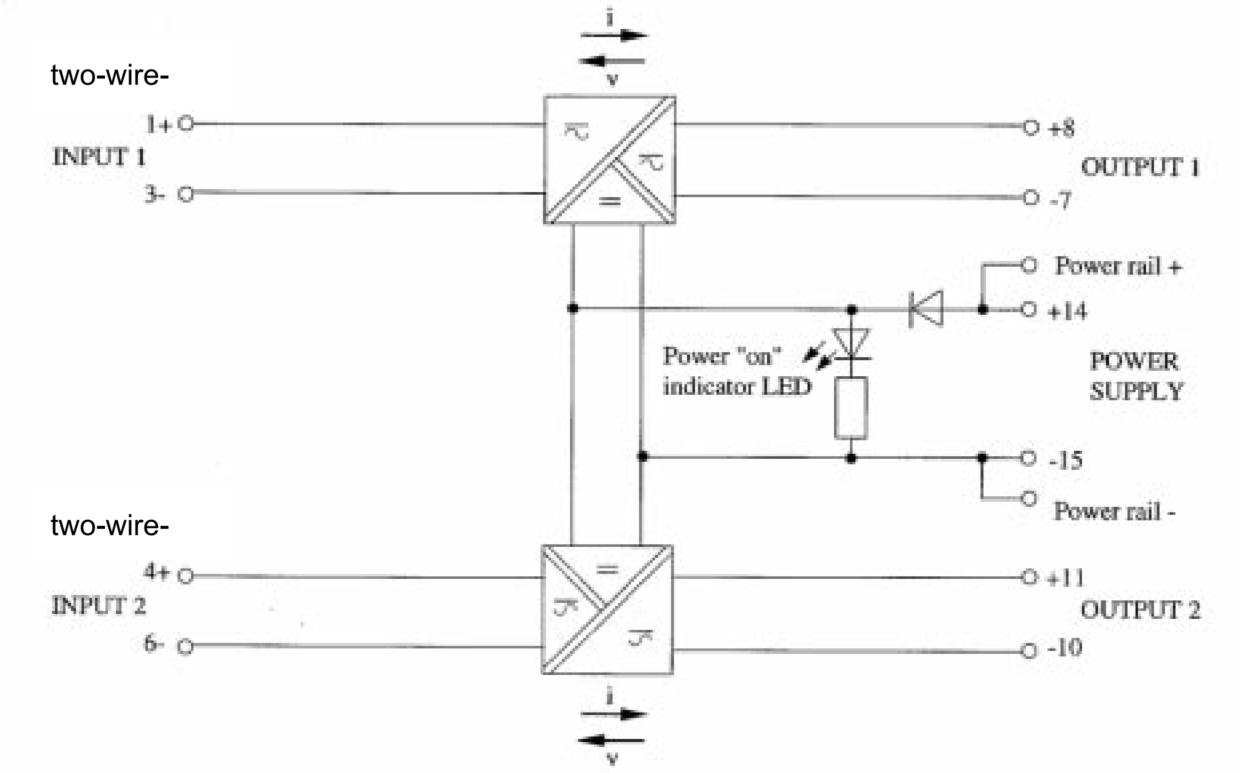


Figure 2: Block diagram of KFD2-STC(V)4-Ex2

3.3 ED2-STC(V)4-Ex2

The ED2-STC(V)4-Ex2 board exists as a 19” euro card where the KFD2-STC(V)4-Ex2 is placed in a DIN RAIL mountable housing. Both modules are identical from a functional point of view.

4 Failure Modes, Effects, and Diagnostics Analysis

4.1 Description of the failure categories

Failures are categorized and defined as follows:

A **fail high** failure (H) is defined as a failure that causes the output signal to go to the maximum output current (> 20mA) or output voltage (> 5V or > 10V).

A **fail low** failure (L) is defined as a failure that causes the output signal to go to the minimum output current (< 4mA) or output voltage (< 1V or < 2V).

A **dangerous** failure (D) is defined as a failure that deviates the output current or voltage by more than 10% of the actual value.

A "don't care" (#) is a failure that has no effect on the safety function of the system or deviates the output current or voltage by not more than 10% of the actual value.

"Not considered" (!) means that this failure mode was not considered.

The failure categories listed above expand on the categories listed in IEC 61508 which are only safe and dangerous, both detected and undetected. The reason for this is that depending on the application a fail low or fail high can either be dangerous or safe and may be detected or undetected depending on the programming of the safety logic solver. Consequently during a Safety Integrity Level (SIL) verification assessment the fail high and fail low categories need to be classified as either safe or dangerous.

4.2 Methodology – FMEDA, Failure rates

4.2.1 FMEDA

A Failure Modes and Effects Analysis (FMEA) is a systematic way to identify and evaluate the effects of different component failure modes, to determine what could eliminate or reduce the change of failure, and to document the system in consideration.

An FMEDA (Failure Mode Effect and Diagnostic Analysis) is an FMEA extension. It combines standard FMEA techniques with extension to identify online diagnostics techniques and the failure modes relevant to safety instrumented system design. It is a technique recommended to generate failure rates for each important category (safe detected, safe undetected, dangerous detected, dangerous undetected, fail high, fail low) in the safety models. The format for the FMEDA is an extension of the standard from MIL STD 1629A, Failure Modes and Effects Analysis.

4.2.2 Failure rates

The failure rate data used by *exida.com* in this FMEDA are from the Siemens SN 29500 failure rate database. The rates were chosen in a way that is appropriate for safety integrity level verification calculations. It is expected that actual field failure results with average environmental stress will be superior to the results predicted by these numbers.

The user of these numbers is responsible for determining their applicability to any particular environment. Accurate plant specific data is preferable to general industry average data. Industrial plant sites with high levels of stress must use failure rate data that is adjusted to a higher value to account for the specific conditions of the plant.

4.2.3 Assumption

The following assumptions have been made during the Failure Modes, Effects, and Diagnostic Analysis of the smart transmitter isolator boards.

Failure rates are constant, wear out mechanisms are not included.

Propagation of failures is not relevant.

All component failure modes are known.

The repair time after a safe failure is 8 hours.

The average temperature over a long period of time is 40°C.

The stress levels are average for an industrial environment.

All modules are operated in the low demand mode of operation.

The application program in the safety logic solver is constructed in such a way that fail low and fail high failures are detected regardless of the effect, safe or dangerous, on the safety function.

5 Results of the assessment

exida.com did the FMEDAs together with Pepperl+Fuchs.

The two channels on each module should not be used for one safety function as they contain common components.

For the calculation of the Safe Failure Fraction (SFF) the following has to be noted:

$_{\text{total}}$ consists of the sum of all component failure rates. This means:

$_{\text{total}} = {}_{\text{safe}} + {}_{\text{dangerous}} + {}_{\text{don't care}}$[4] $+ {}_{\text{not considered}}$[5].

SFF = 1 – $_{\text{du}}$[6] / $_{\text{total}}$

The reason for considering also the “not considered” failure rate for the calculation of the SFF is that the SFF is a measure for the effectiveness of the implemented diagnostic and the percentage of known “safe” failures against all possible component failures.

exida.com estimated for the PFD calculation the effect of the “not considered” failures as 50% “safe” failures and 50% “dangerous” failures.

[4] These are all failures that have no impact on the safety function. The behavior of the system is neither dangerous nor safe.

[5] This is the failure rate of failure modes that were not considered.

[6] This is the failure rate of all dangerous undetected failures.

For the FMEDAs the following failure modes and below mentioned distributions were used.

Resistor / Varistor

Failure Mode	Distribution (in %)
Short	5
Open	59
Drift	36

Capacitor

Failure Mode	Distribution (in %)
Short	80
Open	20

Universal Diode

Failure Mode	Distribution (in %)
Short	49
Open	36
Drift	15

Schottky Diode

Failure Mode	Distribution (in %)
Short	50
Open	50

Zener Diode

Failure Mode	Distribution (in %)
Short	20
Open	45
Drift	35

Integrated Circuit

Failure Mode	Distribution (in %)
Short	17
Open	17
Stuck-at-1	17
Stuck-at-0	17
Drift	17

Fuse

Failure Mode	Distribution (in %)
Short	50
Premature open	50

Inductivity

Failure Mode	Distribution (in %)
Short	50
Open	50

Transformer

Failure Mode	Distribution (in %)
Short	50
Open	50

Transistor

Failure Mode	Distribution (in %)
Short CE	50
Short CB	10
Short EB	10
Open CE	25
1/10 beta; current gain	5

FET MOS

Failure Mode	Distribution (in %)
Short DS	30
Open DS	10
Floating gate	30
Gate leakage	15
1/10 gain	15

Logic CMOS

Failure Mode	Distribution (in %)
Stuck-at-1	10
Stuck-at-0	10
Short	20
Open	60

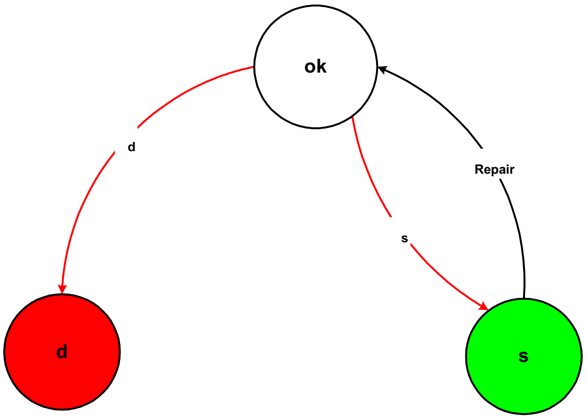
Operational amplifier

Failure Mode	**Distribution (in %)**
Output stuck-at-1	25
Output stuck-at-0	25
Wrong output signal	50

For the calculation of the PFD the following Markov model for a 1oo1 system was used. As there are no explicit on-line diagnostics, no state “dd” – dangerous detected is required.

Also the formula described in IEC 61508-6 (PFD_{AVG} = $_{dangerous}$ (1/2 $T_{[Proof]}$ + $T_{[Repair]}$) can be used to calculate the results.

The proof time was changed using CARMS as a simulation tool. The results are documented in the following sections.



Abbreviations:

d	One channel has failed dangerous
s	One channel has failed safe
$_{du}$	Failure rate of dangerous failures of one channel
$_{s}$	Failure rate of safe failures of one channel
T_{Repair}	Repair time
$_{Repair}$	Repair rate (= 1/T_{Repair})

Figure 3: Markov model

5.1 KFD2-STC(V)4-… three-wire input boards

The FMEDA carried out at the KFD2-STC(V)4-Ex1 board, which is considered to be representative for all KFD2-STC(V)4-… three-wire input boards, leads to the following failure rates:

Current source and sink version:

$_{\text{total}}$ = 4,05E-07 1/h

$_{\text{don't care}}$ = 2,11E-07 1/h

$_{\text{not considered}}$ = 3,63E-09 1/h

Under the assumptions described in section 4.2.3 and 5 the SFF was calculated depending on whether fail low / fail high was considered to be dangerous or safe to:

Failure Categories	safe	dangerous	SFF
Fail low (L) = Safe Fail High (H) = Safe	3,68E-07 1/h	3,64E-08 1/h	91,00 %
Fail low (L) = Safe Fail High (H) = Dangerous	3,54E-07 1/h	5,08E-08 1/h	87,44 %
Fail low (L) = Dangerous Fail High (H) = Safe	2,27E-07 1/h	1,78E-07 1/h	56,04 %
Fail low (L) = Dangerous Fail High (H) = Dangerous	2,12E-07 1/h	1,92E-07 1/h	52,48 %

5V and 10V version:

$_{\text{total}}$ = 4,11E-07 1/h

$_{\text{don't care}}$ = 2,14E-07 1/h

$_{\text{not considered}}$ = 3,63E-09 1/h

Under the assumptions described in section 4.2.3 and 5 the SFF was calculated depending on whether fail low / fail high was considered to be dangerous or safe to:

Failure Categories	safe	dangerous	SFF
Fail low (L) = Safe Fail High (H) = Safe	3,75E-07 1/h	3,64E-08 1/h	91,13 %
Fail low (L) = Safe Fail High (H) = Dangerous	3,60E-07 1/h	5,11E-08 1/h	87,57 %
Fail low (L) = Dangerous Fail High (H) = Safe	2,31E-07 1/h	1,80E-07 1/h	56,17 %
Fail low (L) = Dangerous Fail High (H) = Dangerous	2,16E-07 1/h	1,95E-07 1/h	52,61 %

As there are only minor differences between the current and the voltage version, the PFD calculation was based on the failure rates for the voltage version as this version represents the worst case.

The PFD was calculated for three different proof times using the Markov model as described in Figure 3.

Failure Categories	T[Proof] = 1 year	T[Proof] = 2 years	T[Proof] = 5 years
Fail low (L) = Safe Fail High (H) = Safe	**PFD_{AVG} = 1.6E-04**	**PFD_{AVG} = 3.2E-04**	**PFD_{AVG} = 8.0E-04**
Fail low (L) = Safe Fail High (H) = Dangerous	**PFD_{AVG} = 2.2E-04**	**PFD_{AVG} = 4.5E-04**	**PFD_{AVG} = 1.1E-03**
Fail low (L) = Dangerous Fail High (H) = Safe	**PFD_{AVG} = 7.9E-04**	**PFD_{AVG} = 1.6E-03**	**PFD_{AVG} = 3.9E-03**
Fail low (L) = Dangerous Fail High (H) = Dangerous	**PFD_{AVG} = 8.6E-04**	**PFD_{AVG} = 1.7E-03**	**PFD_{AVG} = 4.3E-03**

The boxes marked in yellow (🟨) mean that the calculated PFD values are within the allowed range for SIL 2 according to table 2 of IEC 61508-1 but do not fulfill the requirement to not claim more than 10% of this range, i.e. to be better than or equal to 10^{-3}. The boxes marked in green (🟩) mean that the calculated PFD values fulfill this requirement to be better than 10^{-3}.

The following figure shows the result of the PFD calculation for T[Proof] = 1 year and fail low and fail high considered to be safe.

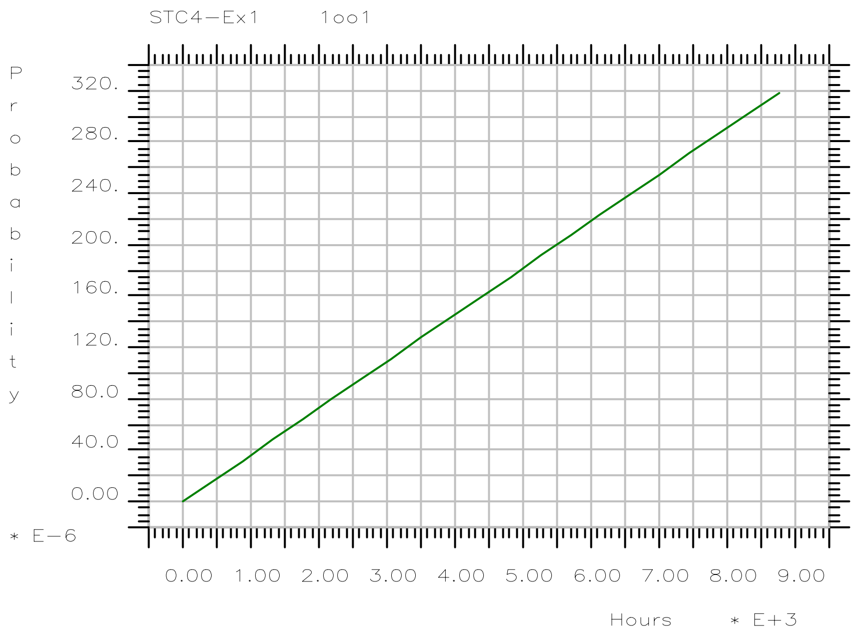


Figure 4: PFD for T[Proof] = 1 year and fail low and fail high considered to be safe

5.2 KFD2-STC(V)4-… and ED2-STC(V)4-… two-wire input boards

The FMEDA carried out at the KFD2-STC(V)4-Ex2 board, which is considered to be representative for all KFD2-STC(V)4-… and ED2-STC(V)4-… two-wire input boards, leads to the following failure rates:

Current source and sink version:

$_{\text{total}}$ = 3,79E-07 1/h

$_{\text{don't care}}$ = 1,97E-07 1/h

$_{\text{not considered}}$ = 3,63E-09 1/h

Under the assumptions described in section 4.2.3 and 5 the SFF was calculated depending on whether fail low / fail high was considered to be dangerous or safe to:

Failure Categories	safe	dangerous	SFF
Fail low (L) = Safe Fail High (H) = Safe	3,42E-07 1/h	3,64E-08 1/h	90,39 %
Fail low (L) = Safe Fail High (H) = Dangerous	3,28E-07 1/h	5,08E-08 1/h	86,58 %
Fail low (L) = Dangerous Fail High (H) = Safe	2,13E-07 1/h	1,66E-07 1/h	56,27 %
Fail low (L) = Dangerous Fail High (H) = Dangerous	1,99E-07 1/h	1,80E-07 1/h	52,47 %

5V and 10V version:

$_{\text{total}}$ = 3,79E-07 1/h

$_{\text{don't care}}$ = 1,97E-07 1/h

$_{\text{not considered}}$ = 3,63E-09 1/h

Under the assumptions described in section 4.2.3 and 5 the SFF was calculated depending on whether fail low / fail high was considered to be dangerous or safe to:

Failure Categories	safe	dangerous	SFF
Fail low (L) = Safe Fail High (H) = Safe	3,43E-07 1/h	3,64E-08 1/h	90,39 %
Fail low (L) = Safe Fail High (H) = Dangerous	3,28E-07 1/h	5,11E-08 1/h	86,53 %
Fail low (L) = Dangerous Fail High (H) = Safe	2,14E-07 1/h	1,66E-07 1/h	56,31 %
Fail low (L) = Dangerous Fail High (H) = Dangerous	1,99E-07 1/h	1,80E-07 1/h	52,45 %

As there are only minor differences between the current and the voltage version, the PFD calculation was based on the failure rates for the voltage version as this version represents the worst case.

The PFD was calculated for three different proof times using the Markov model as described in Figure 3.

Failure Categories	T[Proof] = 1 year	T[Proof] = 2 years	T[Proof] = 5 years
Fail low (L) = Safe Fail High (H) = Safe	PFD_{AVG} = 1.6E-04	PFD_{AVG} = 3.2E-04	PFD_{AVG} = 8.0E-04
Fail low (L) = Safe Fail High (H) = Dangerous	PFD_{AVG} = 2.2E-04	PFD_{AVG} = 4.5E-04	PFD_{AVG} = 1.1E-03
Fail low (L) = Dangerous Fail High (H) = Safe	PFD_{AVG} = 7.3E-04	PFD_{AVG} = 1.5E-03	PFD_{AVG} = 3.6E-03
Fail low (L) = Dangerous Fail High (H) = Dangerous	PFD_{AVG} = 7.9E-04	PFD_{AVG} = 1.6E-03	PFD_{AVG} = 3.9E-03

The boxes marked in yellow (🟨) mean that the calculated PFD values are within the allowed range for SIL 2 according to table 2 of IEC 61508-1 but do not fulfill the requirement to not claim more than 10% of this range, i.e. to be better than or equal to 10^{-3}. The boxes marked in green (🟩) mean that the calculated PFD values fulfill this requirement to be better than 10^{-3}.

The following figure shows the result of the PFD calculation for T[Proof] = 5 years and fail low and fail high considered to be safe.

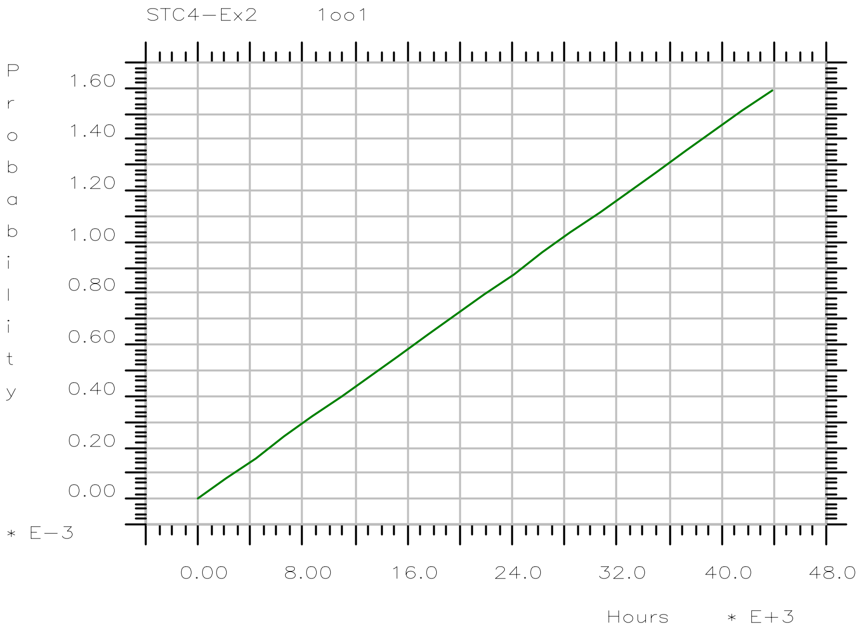


Figure 5: PFD for T[Proof] = 5 years and fail low and fail high considered to be safe

6 Terms and Definitions

FMEDA	Failure Mode Effect and Diagnostic Analysis
Low demand mode	Mode, where the frequency of demands for operation made on a safety-related system is no greater than one per year and no greater than twice the proof test frequency.
PFD	Probability of Failure on Demand
PFD_{AVG}	Average Probability of Failure on Demand
SFF	Safe Failure Fraction summarizes the fraction of failures, which lead to a safe state and the fraction of failures which will be detected by diagnostic measures and lead to a defined safety action.
SIL	Safety Integrity Level

7 Status of the document

7.1 Releases

Version:	V0	
Revision:	R1.0	
Version History:	V0, R1.0:	Initial version, Jun. 28, 2001
	V0, R1.1:	Changes after review by Pepperl+Fuchs, Jul. 19, 2001
	V1, R1.0:	Changes after second review by Pepperl+Fuchs, Jul. 30, 2001
Authors:	Stephan Aschenbrenner	
Review:	V0, R1.0 by Pepperl+Fuchs, Jul. 13, 2001	
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Release status:	Released to Pepperl+Fuchs	