

Pin-Out Table

Termination Board field side		Modules			Termination Board control side		
Module	Channel	IS terminals M1 ... M32	IS terminals SL2 field side	Non-IS terminals SL1 control side	Signal splitter terminals M1 ... M32	System connector XG1	HIMA signal name X-DI 32 01 X-DI 32 04
1	1	1	5a	8a		a1	S1+
		4	5b	7a		b1	DI1+
		2	1a	10a	12		CH1+
		5	1b	9a	15		CH1-
2	2	1	5a	8a		a1	S1+
		4	5b	7a		b2	DI2+
		2	1a	10a	12		CH2+
		5	1b	9a	15		CH2-
3	3	1	5a	8a		a1	S1+
		4	5b	7a		b3	DI3+
		2	1a	10a	12		CH3+
		5	1b	9a	15		CH3-
4	4	1	5a	8a		a1	S1+
		4	5b	7a		b4	DI4+
		2	1a	10a	12		CH4+
		5	1b	9a	15		CH4-
5	5	1	5a	8a		a2	S2+
		4	5b	7a		b5	DI5+
		2	1a	10a	12		CH5+
		5	1b	9a	15		CH5-
6	6	1	5a	8a		a2	S2+
		4	5b	7a		b6	DI6+
		2	1a	10a	12		CH6+
		5	1b	9a	15		CH6-
7	7	1	5a	8a		a2	S2+
		4	5b	7a		b7	DI7+
		2	1a	10a	12		CH7+
		5	1b	9a	15		CH7-
8	8	1	5a	8a		a2	S2+
		4	5b	7a		b8	DI8+
		2	1a	10a	12		CH8+
		5	1b	9a	15		CH8-
9	9	1	5a	8a		a3	S3+
		4	5b	7a		b9	DI9+
		2	1a	10a	12		CH9+
		5	1b	9a	15		CH9-
10	10	1	5a	8a		a3	S3+
		4	5b	7a		b10	DI10+
		2	1a	10a	12		CH10+
		5	1b	9a	15		CH10-
11	11	1	5a	8a		a3	S3+
		4	5b	7a		b11	DI11+
		2	1a	10a	12		CH11+
		5	1b	9a	15		CH11-
12	12	1	5a	8a		a3	S3+
		4	5b	7a		b12	DI12+
		2	1a	10a	12		CH12+
		5	1b	9a	15		CH12-
13	13	1	5a	8a		a4	S4+
		4	5b	7a		b13	DI13+
		2	1a	10a	12		CH13+
		5	1b	9a	15		CH13-
14	14	1	5a	8a		a4	S4+
		4	5b	7a		b14	DI14+
		2	1a	10a	12		CH14+
		5	1b	9a	15		CH14-
15	15	1	5a	8a		a4	S4+
		4	5b	7a		b15	DI15+
		2	1a	10a	12		CH15+
		5	1b	9a	15		CH15-

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Refer to "General Notes Relating to Pepperl+Fuchs Product Information".

Pepperl+Fuchs Group
www.pepperl-fuchs.comUSA: +1 330 486 0002
pa-info@us.pepperl-fuchs.comGermany: +49 621 776 2222
pa-info@de.pepperl-fuchs.comSingapore: +65 6779 9091
pa-info@sg.pepperl-fuchs.com

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Module	Channel	IS terminals M1 ... M32	IS terminals SL2 field side	Non-IS terminals SL1 control side	Signal splitter terminals M1 ... M32	System connector XG1	HIMA signal name X-DI 32 01 X-DI 32 04
16	16	1	5a	8a		a4	S4+
		4	5b	7a		b16	DI16+
		2	1a	10a	12		CH16+
		5	1b	9a	15		CH16-
17	17	1	5a	8a		a5	S5+
		4	5b	7a		b17	DI17+
		2	1a	10a	12		CH17+
		5	1b	9a	15		CH17-
18	18	1	5a	8a		a5	S5+
		4	5b	7a		b18	DI18+
		2	1a	10a	12		CH18+
		5	1b	9a	15		CH18-
19	19	1	5a	8a		a5	S5+
		4	5b	7a		b19	DI19+
		2	1a	10a	12		CH19+
		5	1b	9a	15		CH19-
20	20	1	5a	8a		a5	S5+
		4	5b	7a		b20	DI20+
		2	1a	10a	12		CH20+
		5	1b	9a	15		CH20-
21	21	1	5a	8a		a6	S6+
		4	5b	7a		b21	DI21+
		2	1a	10a	12		CH21+
		5	1b	9a	15		CH21-
22	22	1	5a	8a		a6	S6+
		4	5b	7a		b22	DI22+
		2	1a	10a	12		CH22+
		5	1b	9a	15		CH22-
23	23	1	5a	8a		a6	S6+
		4	5b	7a		b23	DI23+
		2	1a	10a	12		CH23+
		5	1b	9a	15		CH23-
24	24	1	5a	8a		a6	S6+
		4	5b	7a		b24	DI24+
		2	1a	10a	12		CH24+
		5	1b	9a	15		CH24-
25	25	1	5a	8a		a7	S7+
		4	5b	7a		b25	DI25+
		2	1a	10a	12		CH25+
		5	1b	9a	15		CH25-
26	26	1	5a	8a		a7	S7+
		4	5b	7a		b26	DI26+
		2	1a	10a	12		CH26+
		5	1b	9a	15		CH26-
27	27	1	5a	8a		a7	S7+
		4	5b	7a		b27	DI27+
		2	1a	10a	12		CH27+
		5	1b	9a	15		CH27-
28	28	1	5a	8a		a7	S7+
		4	5b	7a		b28	DI28+
		2	1a	10a	12		CH28+
		5	1b	9a	15		CH28-
29	29	1	5a	8a		a8	S8+
		4	5b	7a		b29	DI29+
		2	1a	10a	12		CH29+
		5	1b	9a	15		CH29-
30	30	1	5a	8a		a8	S8+
		4	5b	7a		b30	DI30+
		2	1a	10a	12		CH30+
		5	1b	9a	15		CH30-

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Pepperl+Fuchs Group
www.pepperl-fuchs.comUSA: +1 330 486 0002
pa-info@us.pepperl-fuchs.comGermany: +49 621 776 2222
pa-info@de.pepperl-fuchs.comSingapore: +65 6779 9091
pa-info@sg.pepperl-fuchs.com


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31	31	1	5a	8a		a8	S8+
		4	5b	7a		b31	DI31+
		2	1a	10a	12		CH31+
		5	1b	9a	15		CH31-
32	32	1	5a	8a		a8	S8+
		4	5b	7a		b32	DI32+
		2	1a	10a	12		CH32+
		5	1b	9a	15		CH32-
						a32	reserved
						a31	reserved
						a30	reserved
						a29	reserved

Terminal pin-out	Connector	Pin	Signal name
Power supply	XG2	1	Supply I +
		2	Supply I -
	XG2	3	Supply II +
		4	Supply II -
Volt-free indication output	XG2	5, 6	Fault

Module pin-out (SL1): module 1 ... 32	
V _{cc}	2a (+)
	2b (+)
GND	1a (-)
	1b (-)
Fault	6b

 The loop drawing has to be observed. For information see corresponding data sheet on www.pepperl-fuchs.com.