



# Multiturn absolute encoder BSM58

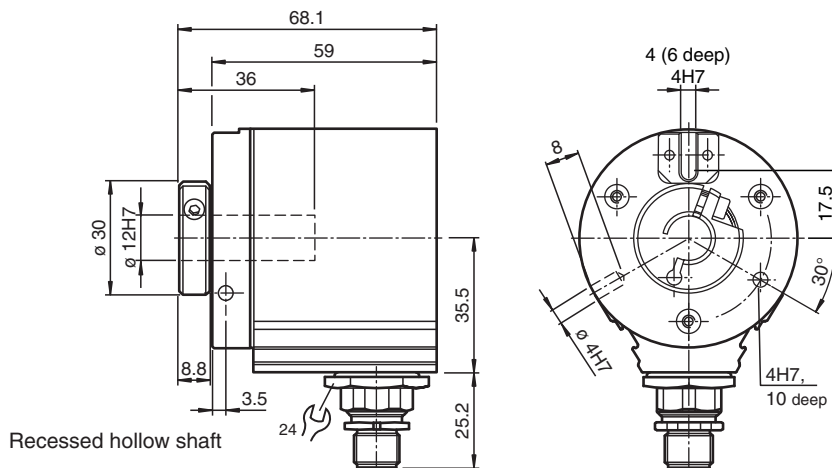
- Industrial standard housing  $\varnothing 58$  mm
- 16 Bit multiturn
- Output code: gray and binary
- Transfer of position data with 4 AS-Interface slaves
- Parameterization and addressing via AS-Interface
- Recessed hollow shaft



## Function

In modern machines and systems, binary sensors and actuators are connected together via AS-Interface. Until now it was necessary to go back to the use of costly conventional wiring when wanting to use absolute encoders. The reason for this was that the handshake mode with the control module of the analogue profile proved to be too slow for positioning tasks. In order to meet the real-time demands of many applications, a multi-slave solution using the BSM58 AS-Interface rotary encoders was created. The position value of 16 Bits in length is transferred within a single cycle via the 4 integrated AS-Interface chips to the master and made available to the PLC. The absolute encoder is mounted directly onto the application shaft, without any coupling. Rotation of the absolute encoder is prevented by a torque rest. This may simply be a slide-in pin that locks in the plastic receptacle integrated into the flange.

## Dimensions



## Technical Data

General specifications	
Detection type	photoelectric sampling
Device type	Multiturn absolute encoder
Electrical specifications	
Operating voltage	$U_B$ 29.5 ... 31.6 V DC
No-load supply current	$I_0$ max. starting current 155 mA , operating current max. 85 mA
Linearity	$\pm 1$ LSB
Output code	programmable, Gray code, binary code
Code course (counting direction)	programmable, cw ascending (clockwise rotation, code course ascending) cw descending (clockwise rotation, code course descending)

Release date: 2022-12-12 Date of issue: 2022-12-12 Filename: t37280\_eng.pdf

Refer to "General Notes Relating to Pepperl+Fuchs Product Information".

Pepperl+Fuchs Group  
www.pepperl-fuchs.com

USA: +1 330 486 0001  
fa-info@us.pepperl-fuchs.com

Germany: +49 621 776 1111  
fa-info@de.pepperl-fuchs.com

Singapore: +65 6779 9091  
fa-info@sg.pepperl-fuchs.com

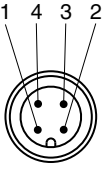
**PF** PEPPERL+FUCHS

## Technical Data

<b>Interface</b>	
Interface type	AS-Interface
<b>Resolution</b>	
Overall resolution	See table, max. 16 Bit
Transfer rate	max. 0.167 MBit/s
Standard conformity	AS-Interface
<b>Connection</b>	
Connector	type V1, M12, 4-pin
<b>Standard conformity</b>	
Degree of protection	DIN EN 60529, IP65
Climatic testing	DIN EN 60068-2-3, no moisture condensation
Emitted interference	EN 61000-6-4:2007
Noise immunity	EN 61000-6-2:2005
Shock resistance	DIN EN 60068-2-27, 100 g, 11 ms
Vibration resistance	DIN EN 60068-2-6, 10 g, 10 ... 2000 Hz
<b>Ambient conditions</b>	
Operating temperature	-20 ... 70 °C (-4 ... 158 °F)
Storage temperature	-25 ... 85 °C (-13 ... 185 °F)
<b>Mechanical specifications</b>	
Material	housing: powder coated aluminum flange: aluminum shaft: stainless steel
Mass	approx. 360 g
Rotational speed	max. 6000 min <sup>-1</sup>
Moment of inertia	30 gcm <sup>2</sup>
Starting torque	≤ 2 Ncm
Tightening torque, fastening screws	max. 1.8 Nm
<b>Shaft load</b>	
Angle offset	1 °
Axial offset	max. 1 mm

**Connection**

Signal	V1 connector, 4-pin	Explanation
AS-Interface +	1	
Reserved	2	Not wired
AS-Interface -	3	
Reserved	4	Not wired

**Interface**

**Addresses**

	Slave A	Slave B	Slave C	Slave D
<b>Preset address</b>	1	2	3	4
<b>IO code</b>	7	0	0	0
<b>ID code</b>	F	F	F	F



When readdressing by means of a bus master or a programming device, it is absolutely essential to assign different addresses to the four integrated AS-Interface chips.

**Parameterization**

**Parameter bits**

The four parameter bits of slave A are used to set the parameters of the rotary encoder. The parameter bits of slave B, C and D are not used.

Status of parameter bit	Slave A			
	P0	P1	P2	P3
0	Gray code	Transfer with flag bits	Descending counting direction for clockwise rotation	Not used
1	Binary code	Transfer without flag bits	Ascending counting direction for clockwise rotation	Not used

**Data bits**

**From the AS-Interface master to the rotary encoder**

Data from the AS-Interface master are transferred to the rotary encoder via slave A, which works bidirectionally. Slaves B, C and D work unidirectionally, i.e. they are incapable of receiving data.

Status of D0/D1 or D2/D3	Slave A			
	D0/D1		D2/D3	
00	Normal mode		Position data are not saved!	
01	Rotary encoder is set to ¼ of the singleturn resolution.		Position data are saved!	
10	Rotary encoder is set to 0.		Position data are saved!	
11	Normal mode		Position data are not saved!	

When a change is made in data bits D2 and D3 from 01 to 10 or vice-versa, position data are resaved in the rotary encoder.

**From the rotary encoder to the AS-Interface master**

Depending on the value of parameter bit P1 of slave A, data transfer to the AS-Interface master takes place with or without flag bits.

P1 = 1: Transfer without flag bits

Slave A				Slave B				Slave C				Slave D			
D0	D1	D2	D3	D0	D1	D2	D3	D0	D1	D2	D3	D0	D1	D2	D3
Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7	Bit 8	Bit 9	Bit 10	Bit 11	Bit 12	Bit 13	Bit 14	Bit 15

Release date: 2022-12-12 Date of issue: 2022-12-12 Filename: 137280\_eng.pdf

Refer to "General Notes Relating to Pepperl+Fuchs Product Information".

P1 = 0: Transfer with flag bits MA, MB, MC, MD

Slave A				Slave B				Slave C				Slave D			
D0	D1	D2	D3	D0	D1	D2	D3	D0	D1	D2	D3	D0	D1	D2	D3
Bit 0	Bit 1	Bit 2	MA	Bit 3	Bit 4	Bit 5	MB	Bit 6	Bit 7	Bit 8	MC	Bit 9	Bit 10	Bit 11	MD

## Operating modes

### Address assignments for the four slaves

The AS-Interface master accesses all slaves one after the other within an AS-Interface cycle in order to transfer output data to slave A or to read in input data from the slaves. The multiturn absolute encoder uses only four AS-Interface chips to transfer the position data that are 16 bits wide, i. e. four slave addresses are assigned.

Since these four slaves are queried one after the other, the data may originate from any one of four different sampling times. To minimise the influence of this effect, sequential addresses (n, n+1, n+2 and n+3) should be assigned to slaves A, B, C and D.

Furthermore, it should be noted that slave A is responsible for controlling the functions of the absolute encoder. If the order of the slaves is changed (D = n, C = n+1, B = n+2, A = n+3), the output word, which is supposed to be transmitted by the function control module of the absolute encoder, will not be transmitted until slaves D, C and B have been read in.

A memory command would thus only take effect for slave A. The command would not take effect for slaves that were already read until the next read cycle. Data consistency would be lost because of the change of order.

### Temporary storage and transfer with flag bits

If individual telegrams of the four slaves to the AS-Interface master suffer interference, it may happen in spite of temporary storage in the rotary encoder that the data that are transferred to the control module do not all originate from the same position data set.

Transferring one flag bit for each slave makes it possible for the control module to check which position data set an individual data set belongs to by comparing the four flag bits. Data bit D2 is used for this purpose.

Example:

Cycle	Slave A Data bit D2	Position data			
		Slave A	Slave B	Slave C	Slave D
1	0	XXX0	XXX0	XXX0	XXX0
2	1	XXX1	XXX1	XXX1	XXX1
3	0	XXX0	XXX0	XXX0	XXX0
4	1	XXX1	XXX1	XXX1	XXX1
etc.					

Bit D2 is influenced by the control module. Bit 4 of the input data corresponds to the value of this bit for each slave.

D2 is set to 0 in cycle 1. If the value of bit 4 of a slave were "1", that value would be derived from another cycle. This is a simple way to recognise data consistency.

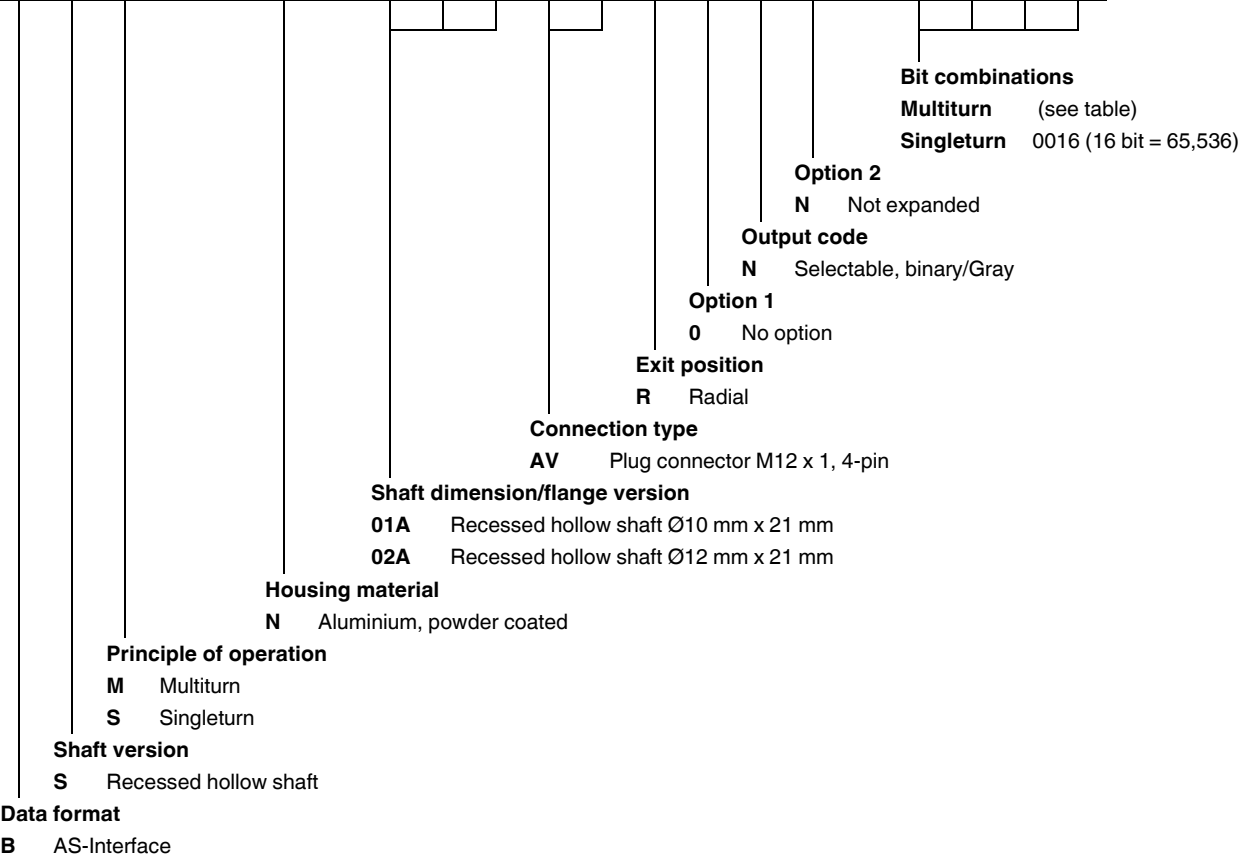
Transferring the flag bits, however, reduces the usable position data from 13 bits to 12. Masking out the fourth bit of each slave increases slightly the effort of putting together the position data set in the control module.

## Resolution of the rotary encoder

Possible combinations of steps per revolution and number of rotations	Without flag bits				With flag bits			
	Number of rotations	Bits	Steps per revolution	Bits	Number of rotations	Bits	Steps per revolution	Bits
8	03	8192	13	not allowed				
16	04	4096	12	2	01	2048	11	
32	05	2048	11	4	02	1024	10	
64	06	1024	10	8	03	512	09	
128	07	512	09	16	04	256	08	
256	08	256	08	32	05	128	07	
512	09	128	07	64	06	64	06	
1024	10	64	06	128	07	32	05	
2048	11	32	05	256	08	16	04	
4096	12	16	04	512	09	8	03	

## Type Code

**Order code**



Release date: 2022-12-12 Date of issue: 2022-12-12 Filename: 137280\_eng.pdf

Refer to "General Notes Relating to Pepperl+Fuchs Product Information".